IN THE CLAIMS:

Please accept amended claims 1 and 18 and new claim 19 as follows:

1. (currently amended) A memory device comprising:

a first memory array having a plurality of first memory cells, wherein each one of the plurality of first memory cells is arranged at an intersection of at least one of a plurality of wordlines, at least one of a plurality of bitlines, and at least one of a plurality of digit lines;

a second memory array having a plurality of second memory cells, wherein each one of the plurality of second memory cells is arranged at an intersection of at least one of the plurality of wordlines, at least one of a first bitline and a second bitline of the plurality of bitlines, and at least one of the plurality of digit lines;

a current providing unit for providing a second current to ~~one of the first bitline and the second~~ a reference bitline in response to a reference voltage; and

a sense amplifier for comparing a first current flowing through one of the plurality of bitlines with the second current.

2. (original) The memory device of claim 1, wherein the current providing unit comprises:

a first current mirror coupled to the first bitline, wherein a current from the first bitline flows through the first current mirror in response to the reference voltage;

a second current mirror coupled to the second bitline, wherein a current from the second bitline flows through the second current mirror in response to the reference voltage; and

a third current mirror for providing half of the sum of the current from the first bitline and the current from the second bitline to the sense amplifier.

3. (original) The memory device of claim 1, wherein each one of the plurality of second memory cells set to a first logic state is coupled to the first bitline and each one of the plurality of second memory cells set to a second logic state is coupled to the second bitline.

4. (original) The memory device of claim 1, further comprising a circuit for clamping down a voltage of a first data line through which the first current is transmitted, and a voltage of a second data line through which the second current is transmitted, to the reference voltage when one of the plurality of wordlines of one of the plurality of first memory cells is enabled.

5. (original) The memory device of claim 1, wherein the first memory cells and the second memory cells are magnetic.

6. (original) The memory device of claim 1, wherein the first current is a target current.

7. (original) The memory device of claim 1, wherein the second current is defined by the expression (i(H)+i(L))/2.

8. (original) The memory device of claim 1, wherein the second current is a reference current.

9. (original) The memory device of claim 1, wherein the first current is compared to the second current to determine a logic state of a predetermined one of the plurality of first memory cells.

10. (original) A memory device comprising:

a plurality of first bitlines and a plurality of second bitlines;

a first memory array having a plurality of first memory cells;

a second memory array having a plurality of second memory cells;

a current providing unit for providing a second current to one of the plurality of second bitlines in response to a reference voltage; and

a sense amplifier for comparing a first current flowing through one of the plurality of first bitlines with the second current.

11. (original) The memory device of claim 10, wherein the current providing unit comprises:

a first current mirror coupled to a first one of the plurality of second bitlines;

a second current mirror coupled to a second one of the plurality of second bitlines; and

a third current mirror for providing half of the sum of a current from the first current mirror and a current from the second current mirror to the sense amplifier.

12. (original) The memory device of claim 10, wherein each one of the plurality of second memory cells set to a first logic state is coupled to a first one of the plurality of second bitlines and each one of the plurality of second memory cells set to a second logic state is coupled to a second one of the plurality of second bitlines.

13. (original) The memory device of claim 10, further comprising a circuit for clamping down a voltage of a line through which the first current is transmitted, and a voltage of a line through which the second current is transmitted, to the reference voltage.

14. (original) The memory device of claim 10, wherein the first memory cells and the second memory cells are magnetic.

15. (original) The memory device of claim 10, wherein the first current is a target current.

16. (original) The memory device of claim 10, wherein the second current is defined by the expression (i(H)+i(L))/2.

17. (original) The memory device of claim 10, wherein the second current is a reference current.

18. (currently amended) The memory device of claim [[1]] 10, wherein the first current is compared to the second current to determine a logic state of a predetermined one of the plurality of first memory cells.

19. (new) A memory device comprising:

a plurality of bitlines intersecting with a plurality of wordlines and a plurality of digit lines to form a plurality of memory cells;

a sense amplifier; and

a current providing unit electrically coupled to the sense amplifier for providing a reference current to the sense amplifier, wherein:

the sense amplifier compares a current flowing through a first one of the plurality of bitlines with the reference current; and

the current providing unit comprises:

a first current mirror coupled to a second one of the plurality of bitlines;

a second current mirror coupled to a third one of the plurality of bitlines; and

a third current mirror for providing the reference current equal to half of the sum of a current from the first current mirror and a current from the second current mirror to the sense amplifier.